



(19)

(11) Publication number:

6

Generated Document.

## PATENT ABSTRACTS OF JAPAN

(21) Application number: **59209821**(51) Intl. Cl.: **G06F 11/34 G06F 13/00**(22) Application date: **08.10.84**

(30) Priority:

(43) Date of application  
publication: **06.05.86**(84) Designated contracting  
states:(71) Applicant: **MITSUBISHI ELECTRI**(72) Inventor: **AKAHORI NOZOMI**

(74) Representative:

### **(54) ERROR ANALYZING SYSTEM OF TERMINAL CONTROLLING DEVICE**

(57) Abstract:

**PURPOSE:** To make an error analysis at set timing without stopping system processing by detecting the preset timing of error analysis in a terminal controlling device, and reading error log trace information by a central processing unit.

**CONSTITUTION:** An error log buffer 5A stores the number of times of errors generated in each interface in which the CPU 1 is connected to a group of terminal units through a terminal equipment 2 by kinds of errors. On the other hand, a trace buffer 5B traces a transmission controlling procedure and stores the information. When reading information of buffers 5A and 5B from a error log trace buffer 5, timing of error analysis is set by a timing setting and timer processing section

14, and the error analyzing operation is controlled by signals from an error analyzing operation controlling section 13. Thus, the content of the buffers 5A and 5B can be read without stopping the operation of the system.

COPYRIGHT: (C)1986,JPO&Japio

